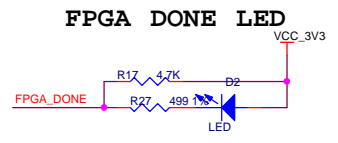
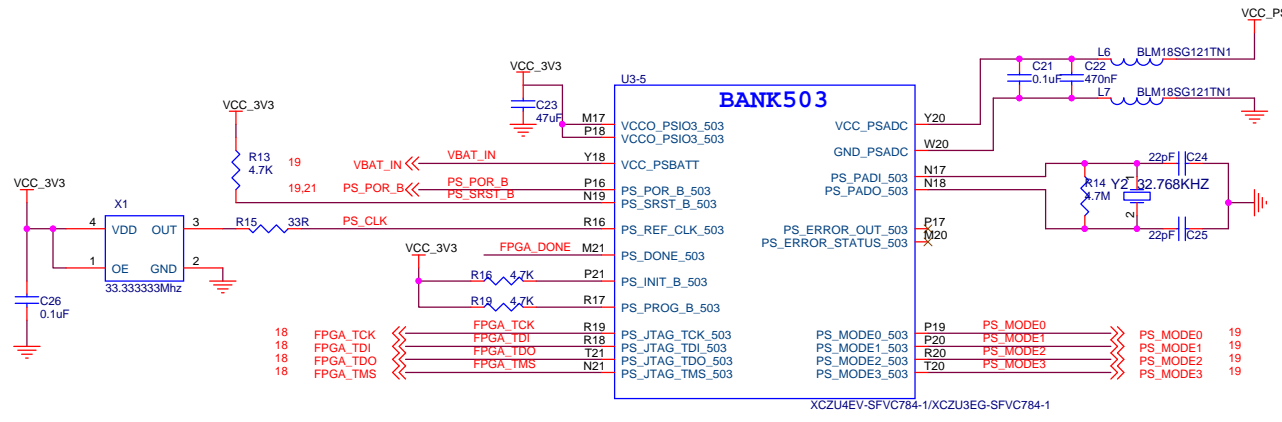
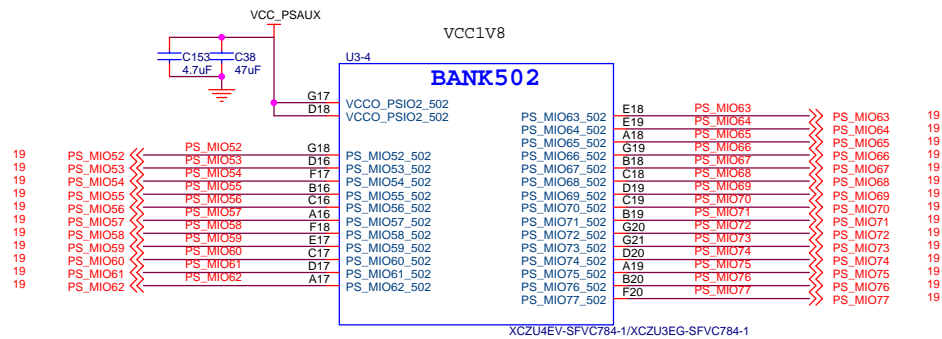
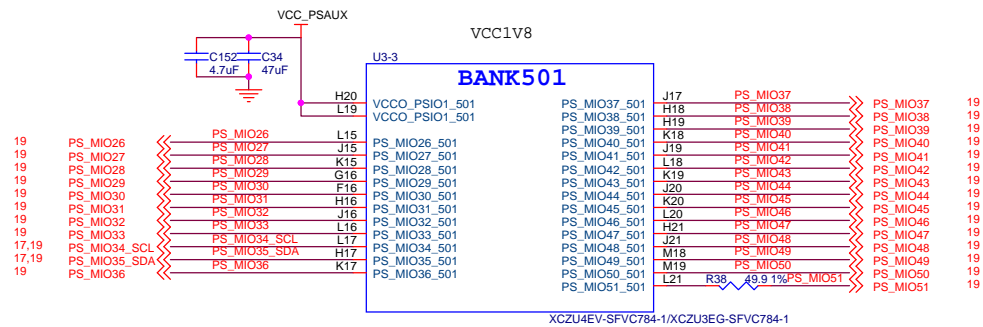
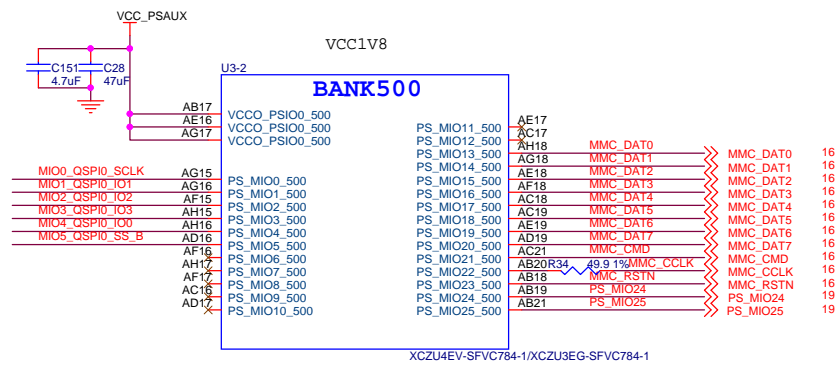
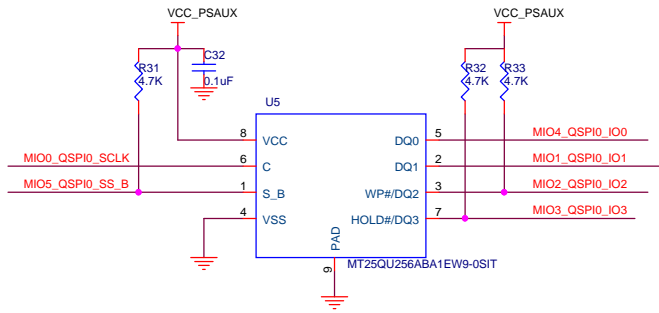
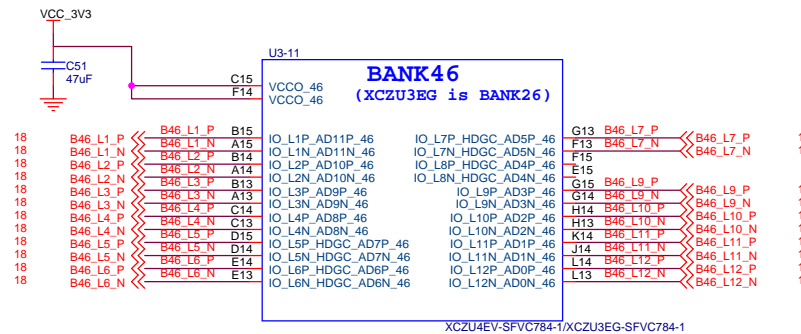
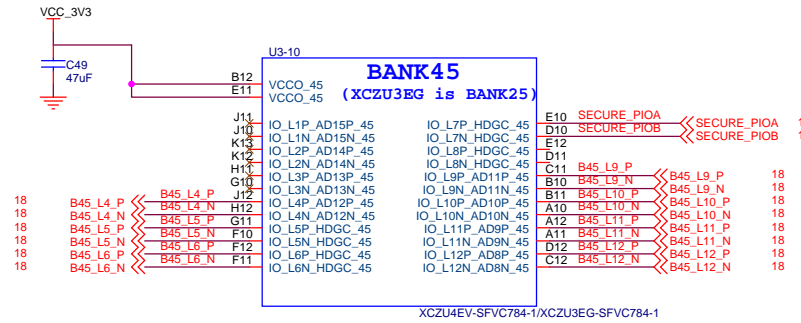
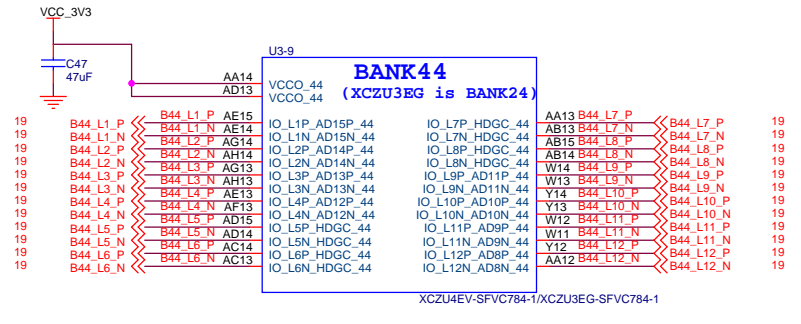
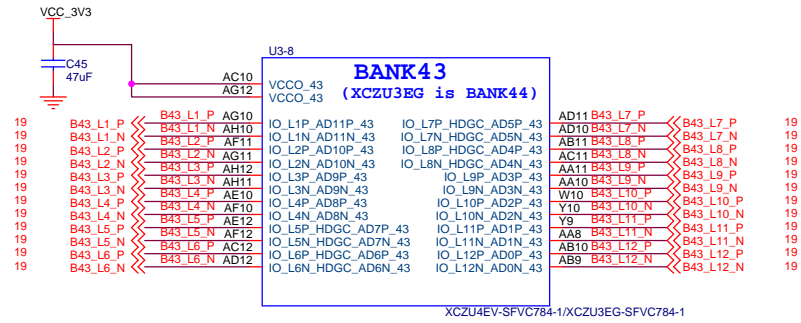


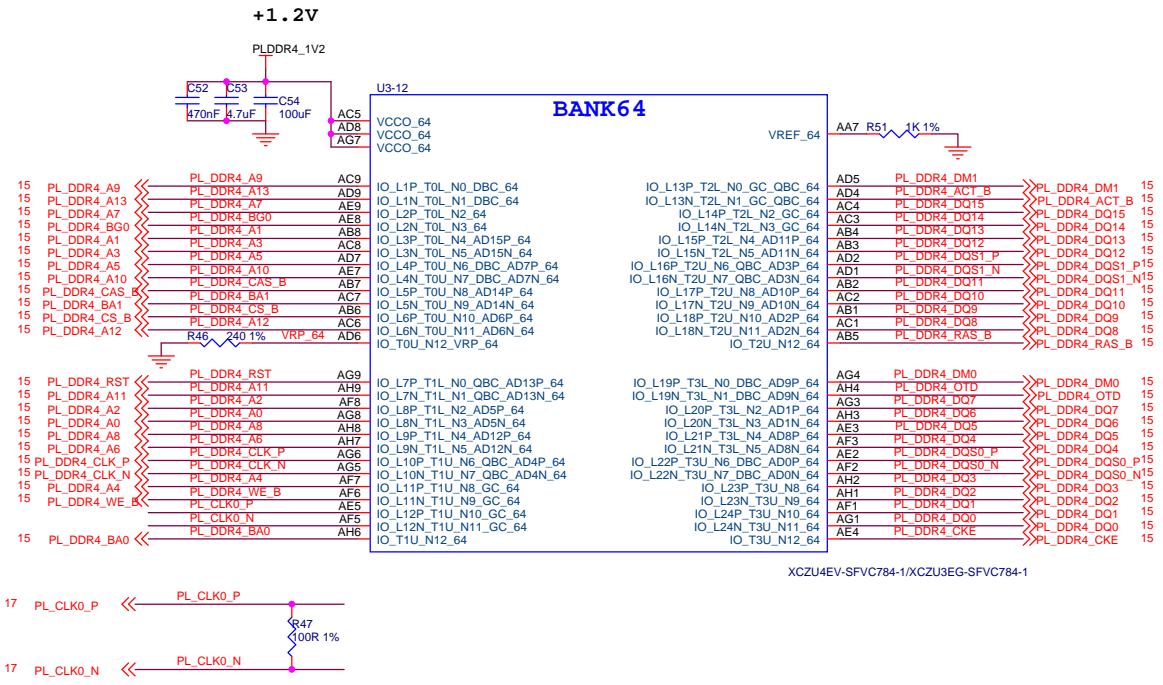
MODE[3:0] BOOT MODE Description

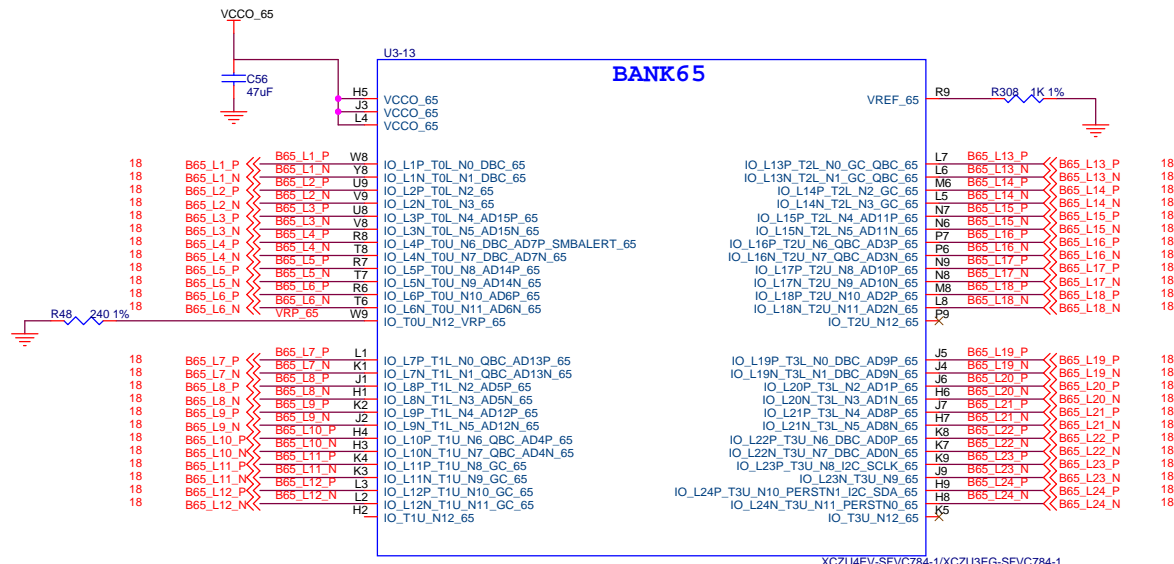
MODE[3:0]	BOOT MODE	Description
0000	PS JTAG	PS JTAG Interface
0001	Quad SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0



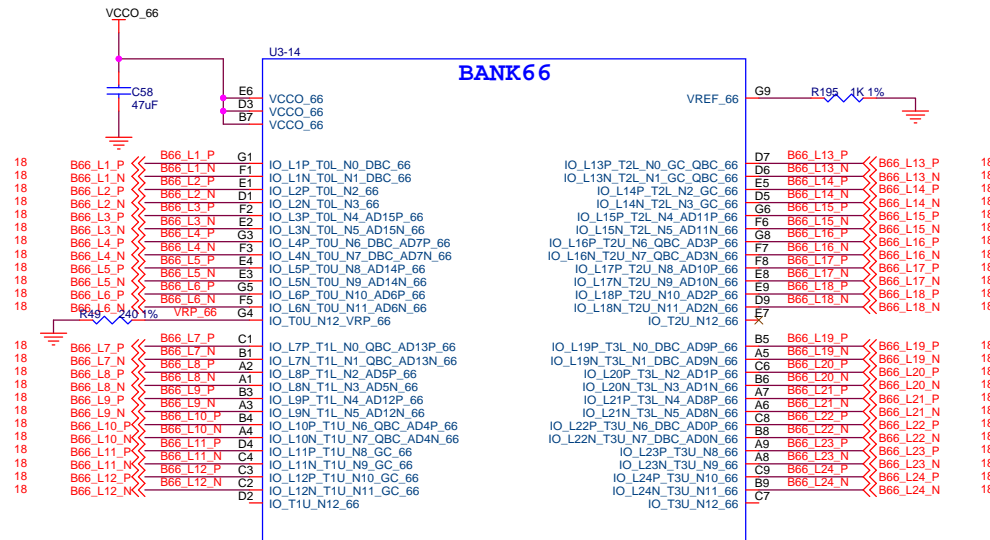




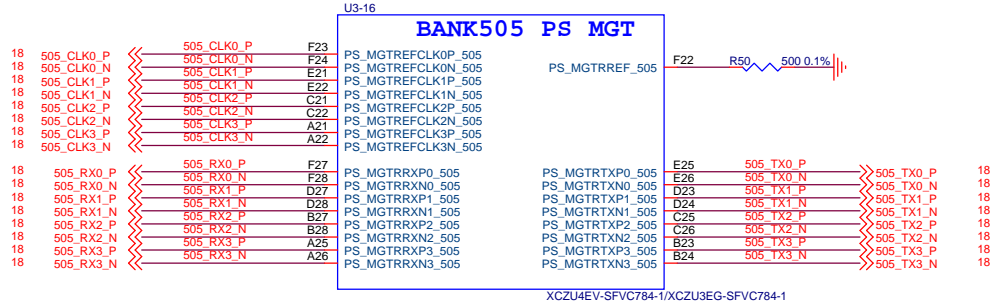


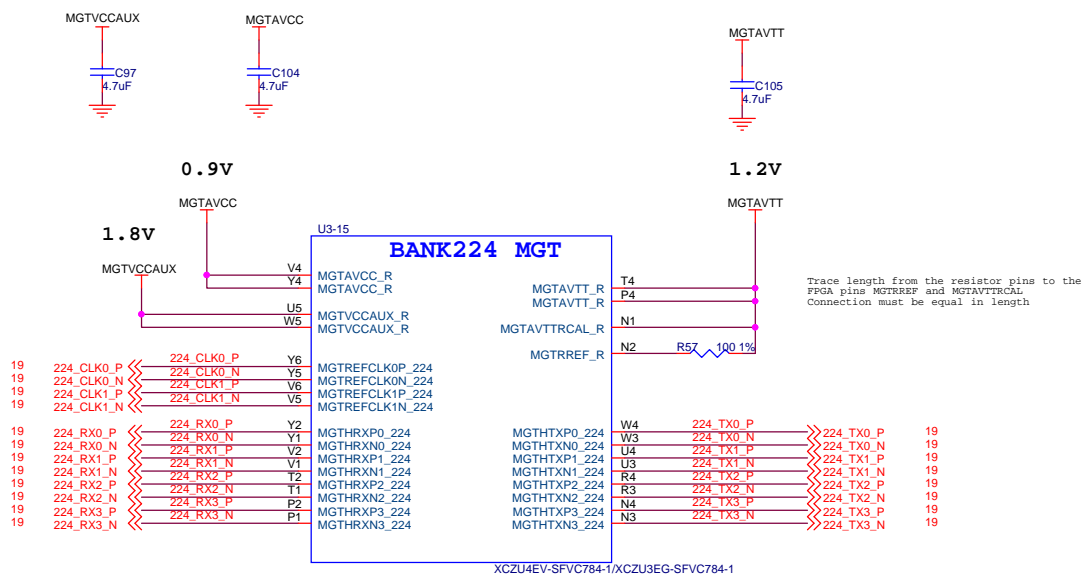


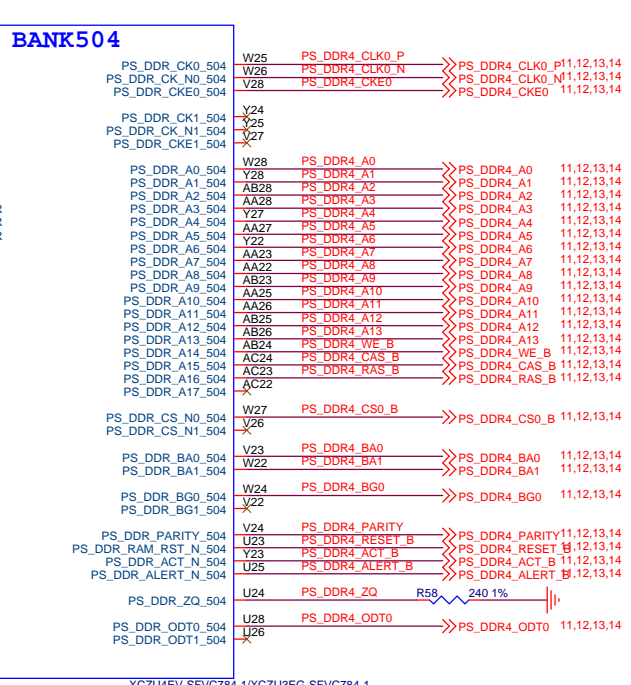
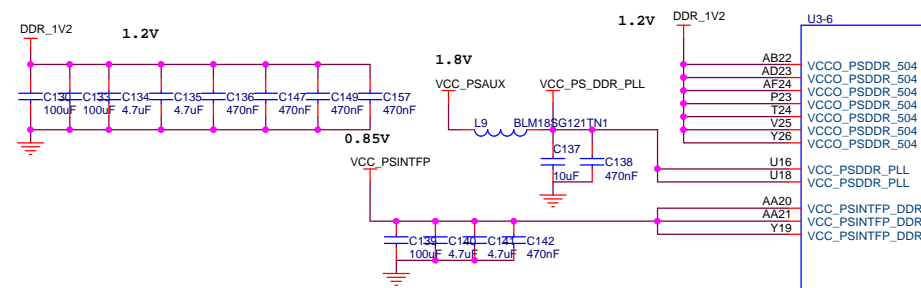
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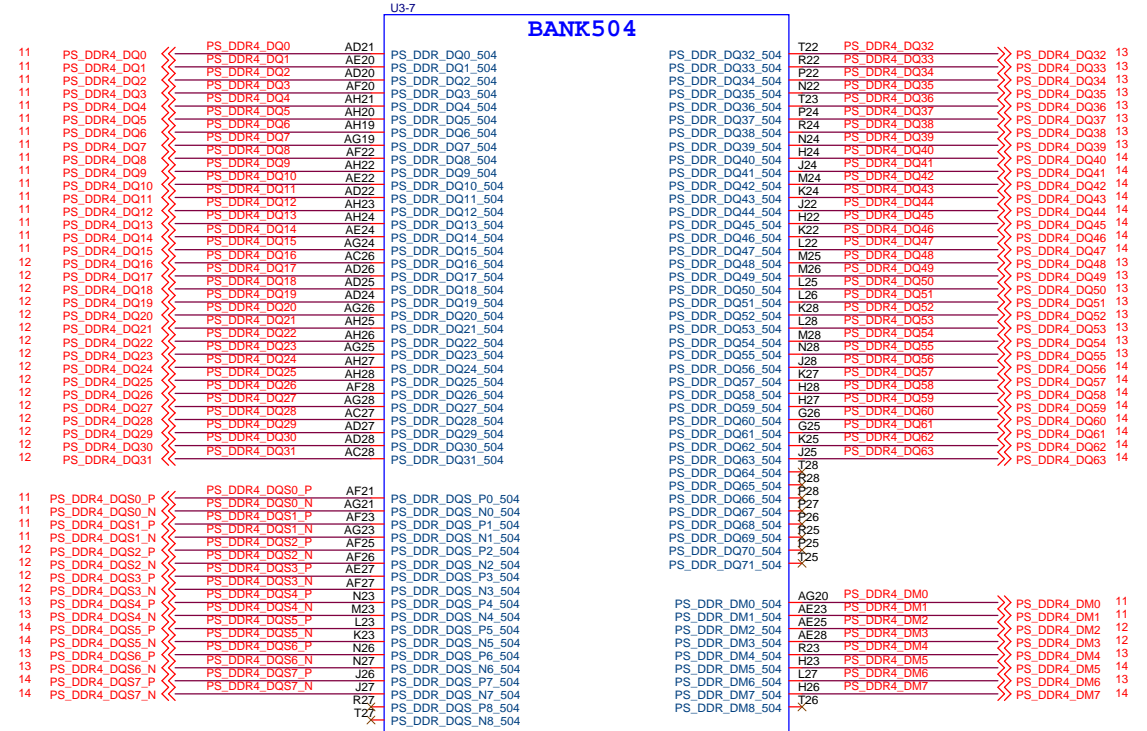
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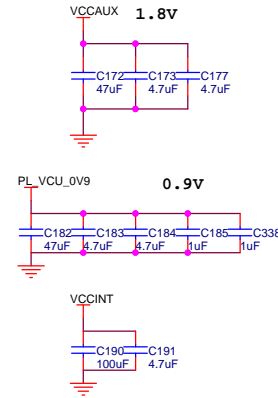
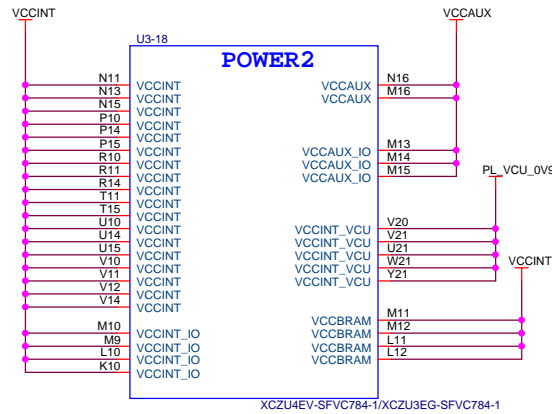
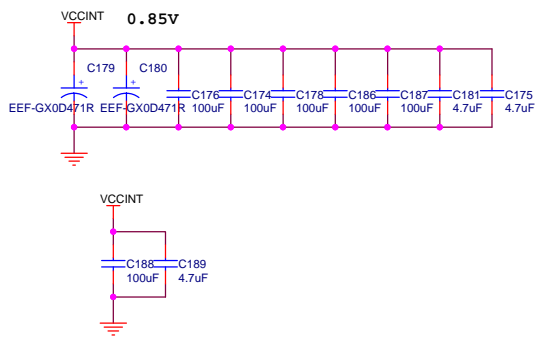
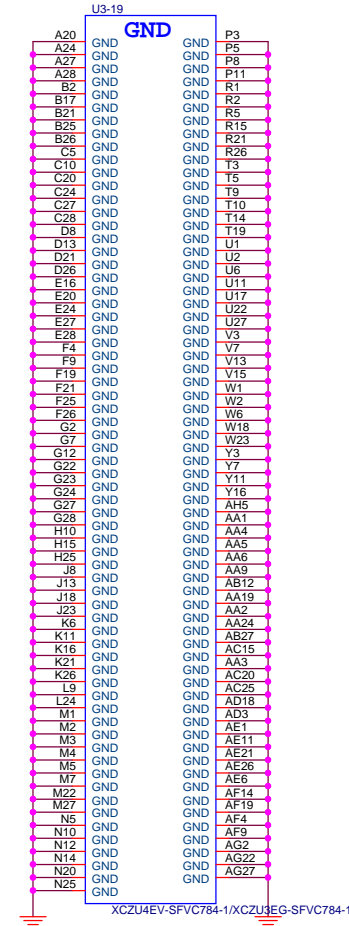
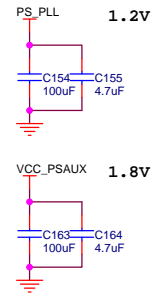
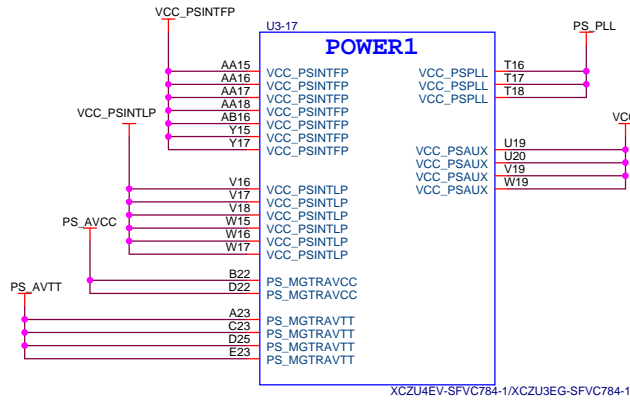
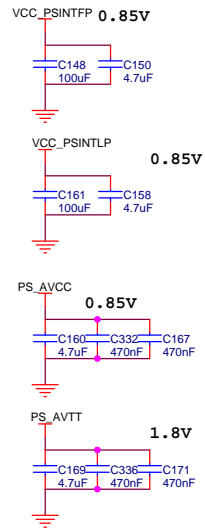
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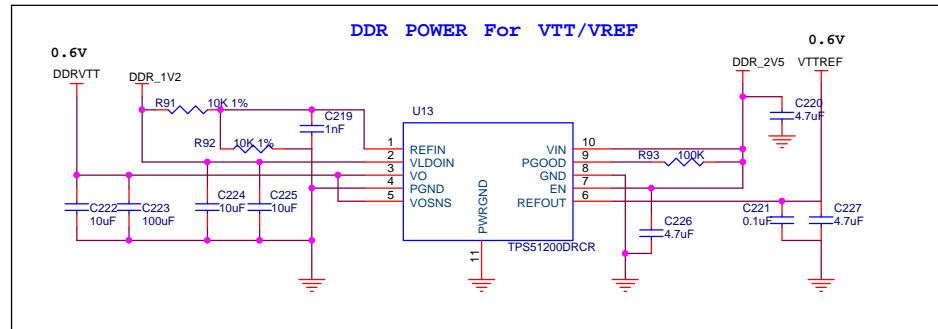
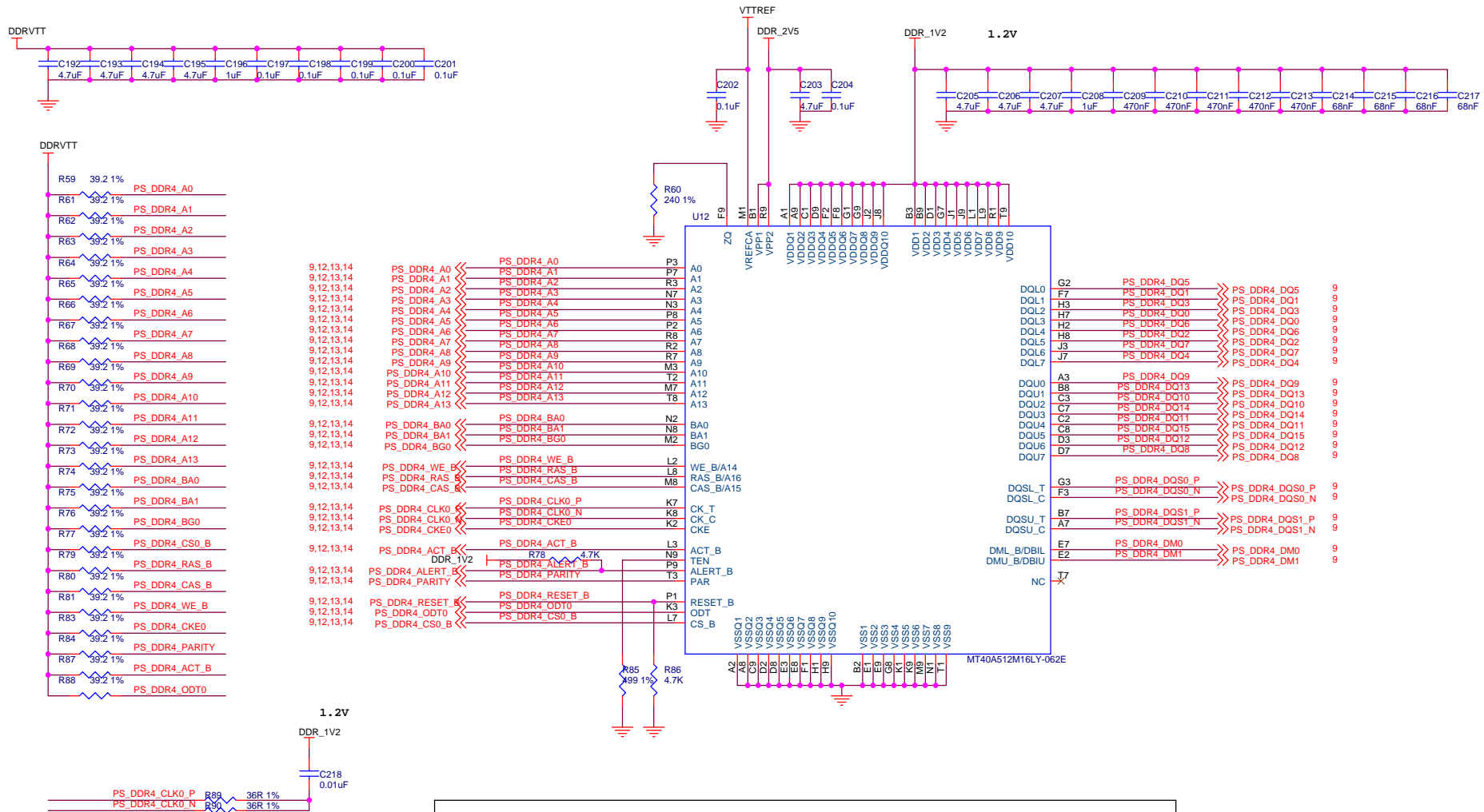
ALINX www.alinx.com

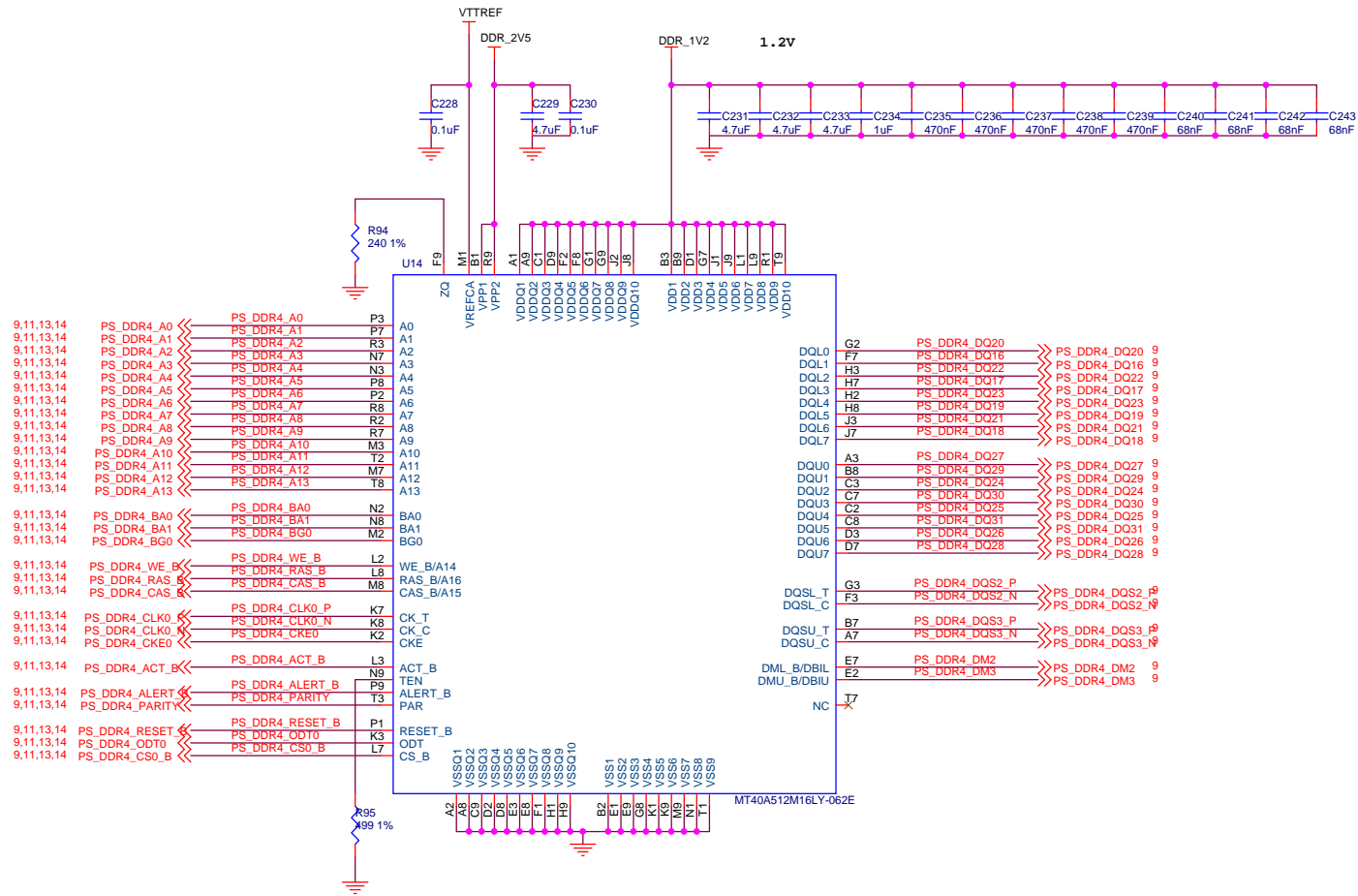
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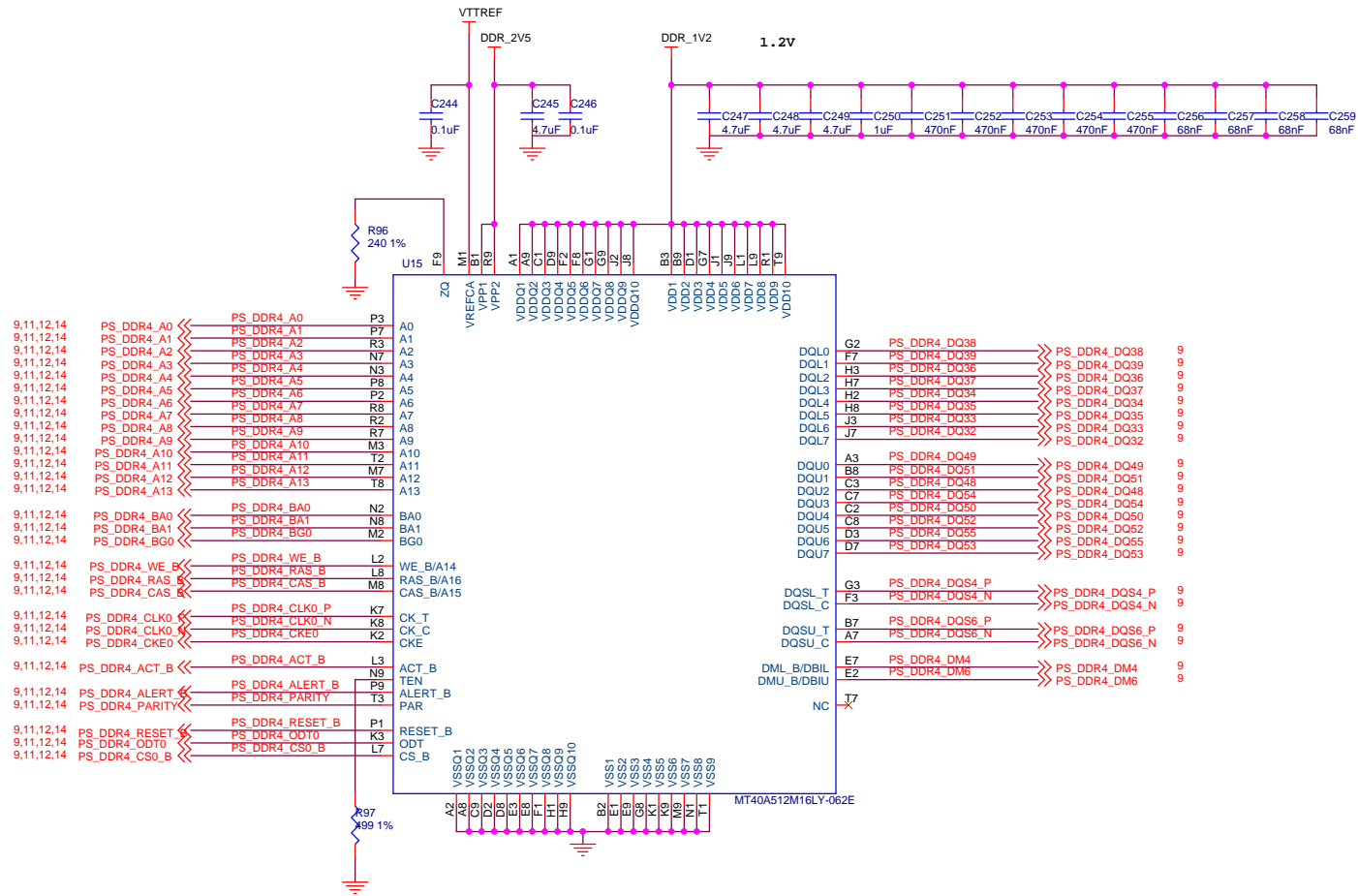
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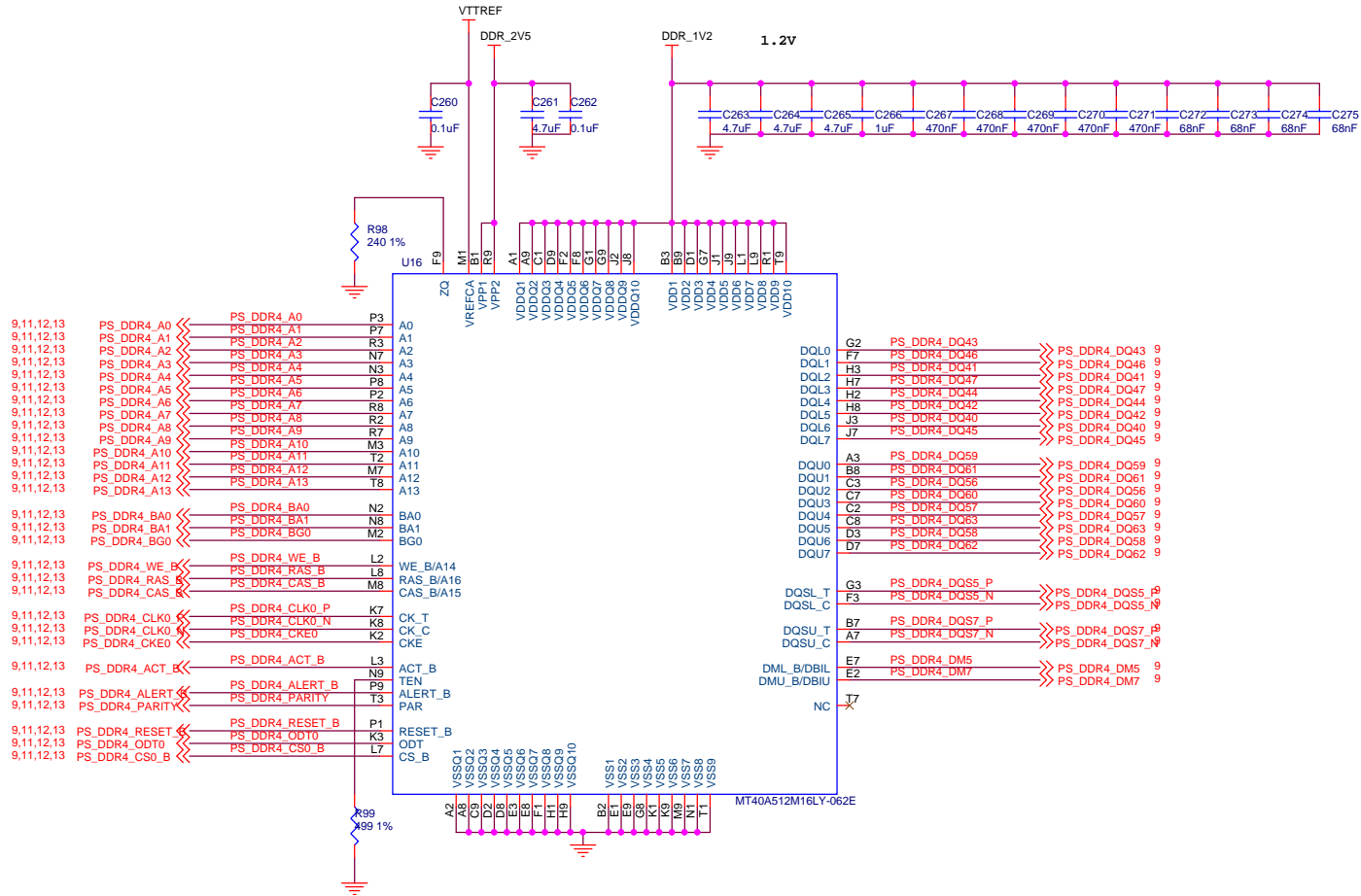
Date: Tuesday, May 11, 2021 Sheet: 9 of 21

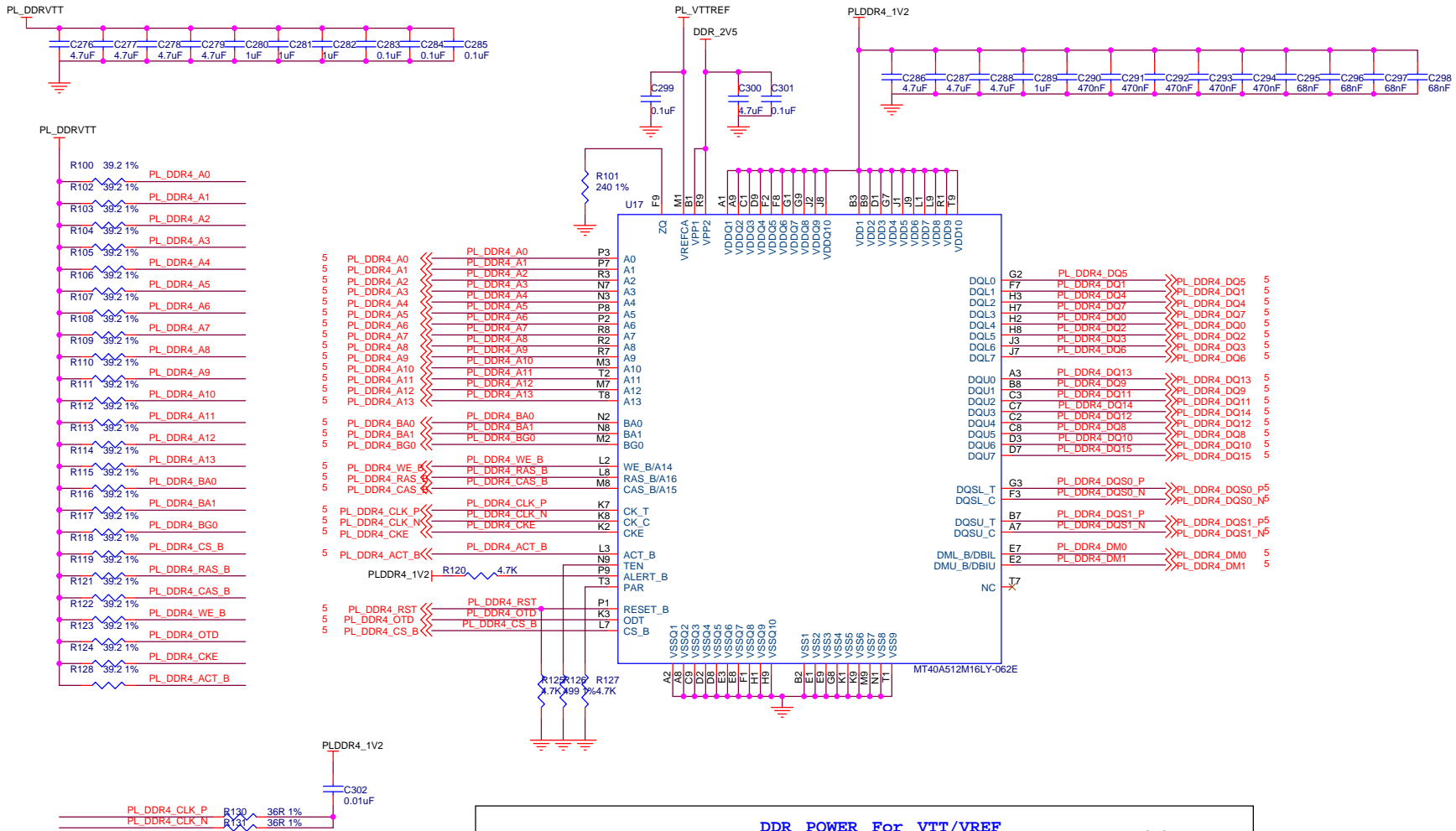




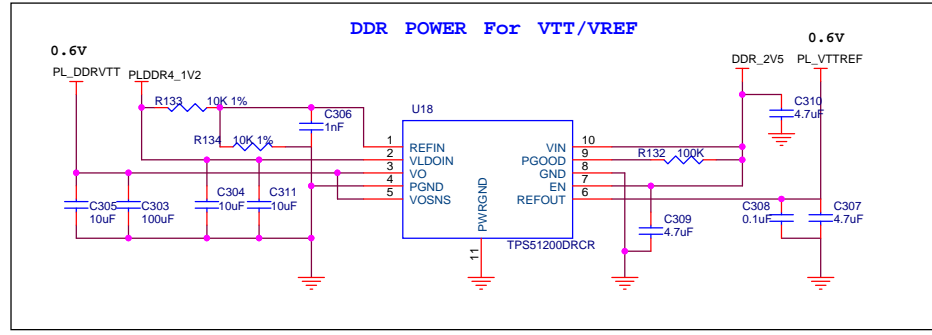


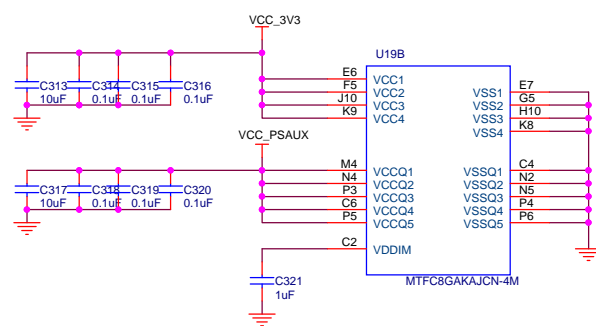
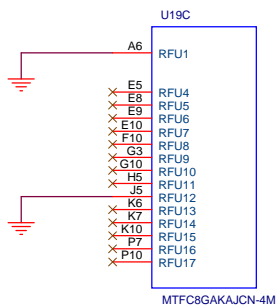
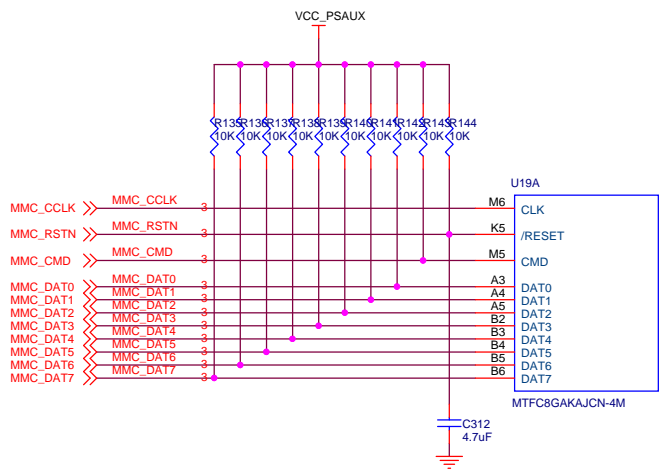
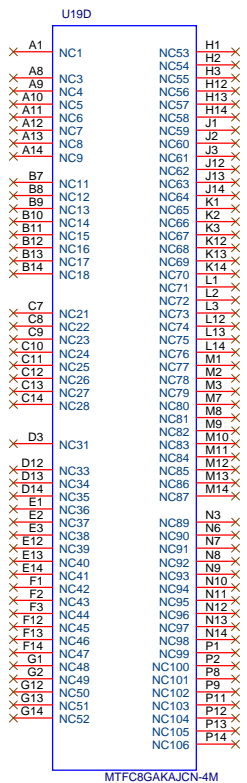






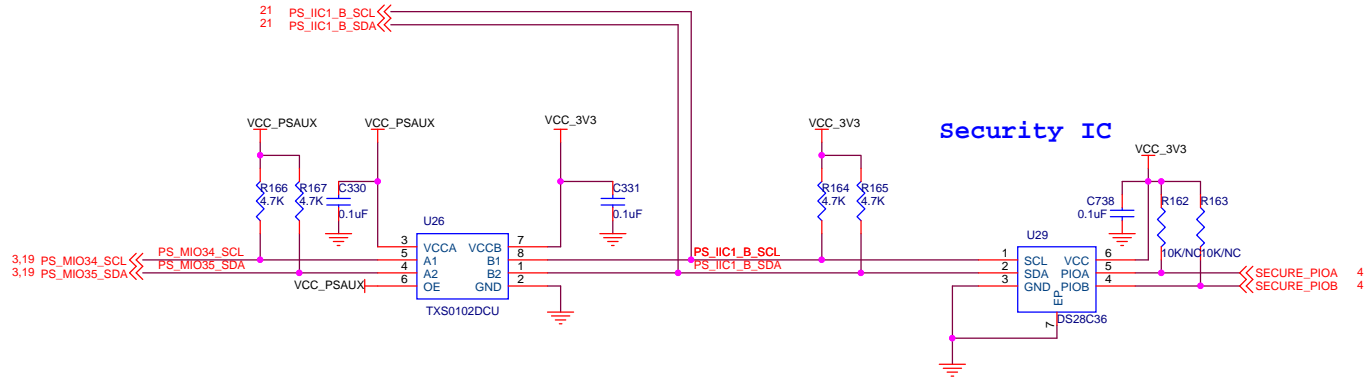
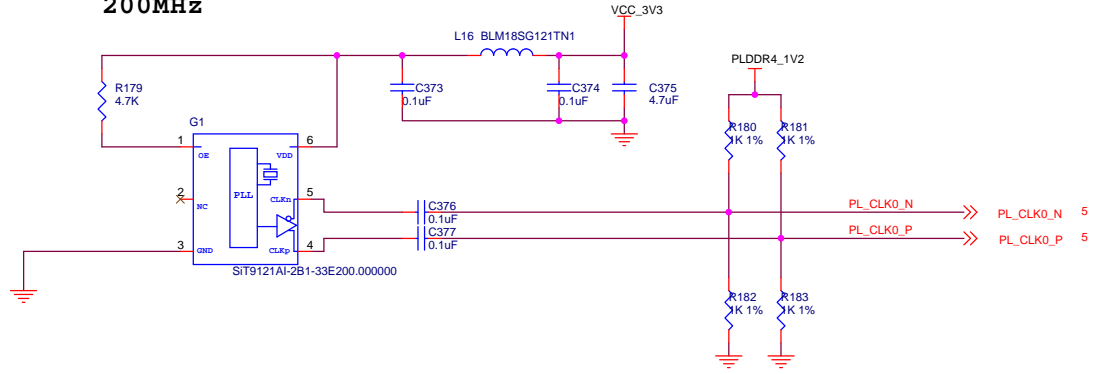
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5	PL_DDR4_A1	PL_DDR4_A1	P7	A1	DQ1	F7	PL_DDR4_DQ1	PL_DDR4_DQ1	5
5	PL_DDR4_A2	PL_DDR4_A2	R3	A2	DQ2	H3	PL_DDR4_DQ2	PL_DDR4_DQ2	5
5	PL_DDR4_A3	PL_DDR4_A3	N7	A3	DQ3	H7	PL_DDR4_DQ3	PL_DDR4_DQ3	5
5	PL_DDR4_A4	PL_DDR4_A4	N3	A4	DQ4	H6	PL_DDR4_DQ4	PL_DDR4_DQ4	5
5	PL_DDR4_A5	PL_DDR4_A5	P8	A5	DQ5	J3	PL_DDR4_DQ5	PL_DDR4_DQ5	5
5	PL_DDR4_A6	PL_DDR4_A6	P2	A6	DQ6	J7	PL_DDR4_DQ6	PL_DDR4_DQ6	5
5	PL_DDR4_A7	PL_DDR4_A7	R8	A7	DQ7	A3	PL_DDR4_DQ7	PL_DDR4_DQ7	5
5	PL_DDR4_A8	PL_DDR4_A8	R2	A8	DQ8	B8	PL_DDR4_DQ8	PL_DDR4_DQ8	5
5	PL_DDR4_A9	PL_DDR4_A9	R7	A9	DQ9	C3	PL_DDR4_DQ9	PL_DDR4_DQ9	5
5	PL_DDR4_A10	PL_DDR4_A10	M3	A10	DQ10	C7	PL_DDR4_DQ10	PL_DDR4_DQ10	5
5	PL_DDR4_A11	PL_DDR4_A11	T2	A11	DQ11	C2	PL_DDR4_DQ11	PL_DDR4_DQ11	5
5	PL_DDR4_A12	PL_DDR4_A12	M7	A12	DQ12	C8	PL_DDR4_DQ12	PL_DDR4_DQ12	5
5	PL_DDR4_A13	PL_DDR4_A13	T8	A13	DQ13	D3	PL_DDR4_DQ13	PL_DDR4_DQ13	5
5	PL_DDR4_BA0	PL_DDR4_BA0	N2	BA0	DQ14	E7	PL_DDR4_DM0	PL_DDR4_DM0	5
5	PL_DDR4_BA1	PL_DDR4_BA1	N8	BA1	DQ15	E2	PL_DDR4_DM1	PL_DDR4_DM1	5
5	PL_DDR4_BG0	PL_DDR4_BG0	M2	BG0	DQ16	I7			
5	PL_DDR4_WE_B	PL_DDR4_WE_B	L2	WE_B/A14	DQ17				
5	PL_DDR4_RAS_B	PL_DDR4_RAS_B	L8	RAS_B/A15					
5	PL_DDR4_CAS_B	PL_DDR4_CAS_B	M8	CAS_B/A15					
5	PL_DDR4_CLK_P	PL_DDR4_CLK_P	K7	CK_T					
5	PL_DDR4_CLK_N	PL_DDR4_CLK_N	K8	CK_C					
5	PL_DDR4_CKE	PL_DDR4_CKE	K2	CKE					
5	PL_DDR4_ACT_B	PL_DDR4_ACT_B	L3	ACT_B					
	PLDDR4_1V2		N9	TEN					
			P9	ALERT_B					
			T3	PAR					
5	PL_DDR4_RST	PL_DDR4_RST	P1	RESET_B					
5	PL_DDR4_OTD	PL_DDR4_OTD	K3	ODT					
5	PL_DDR4_CS_B	PL_DDR4_CS_B	L7	CS_B					





PL SYSTEM CLOCK

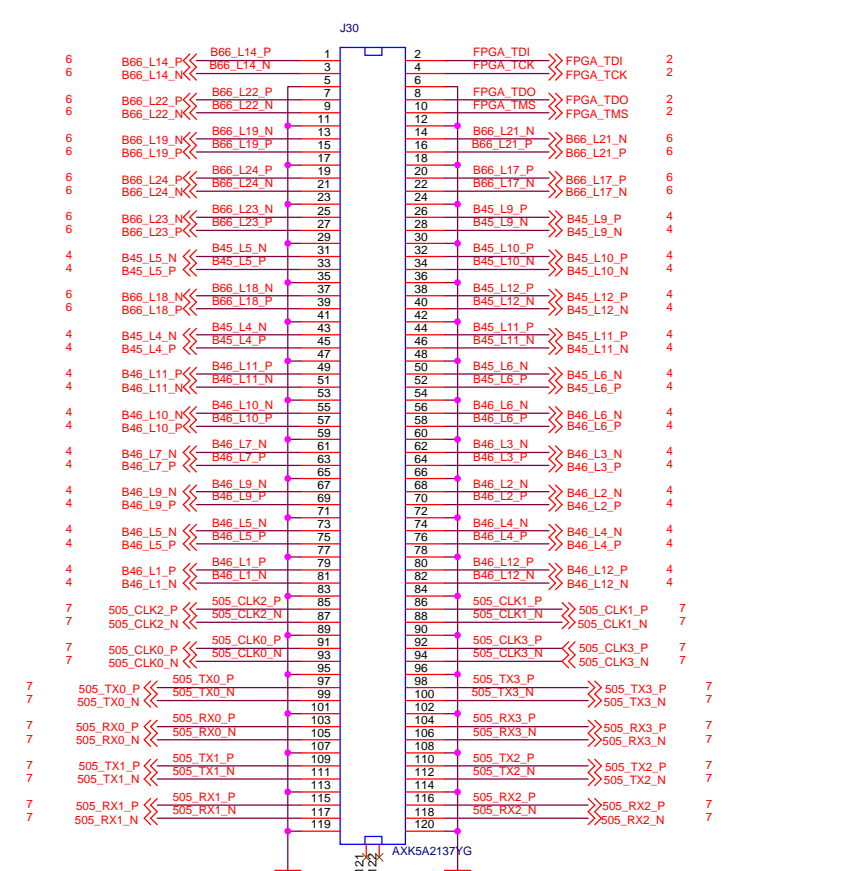
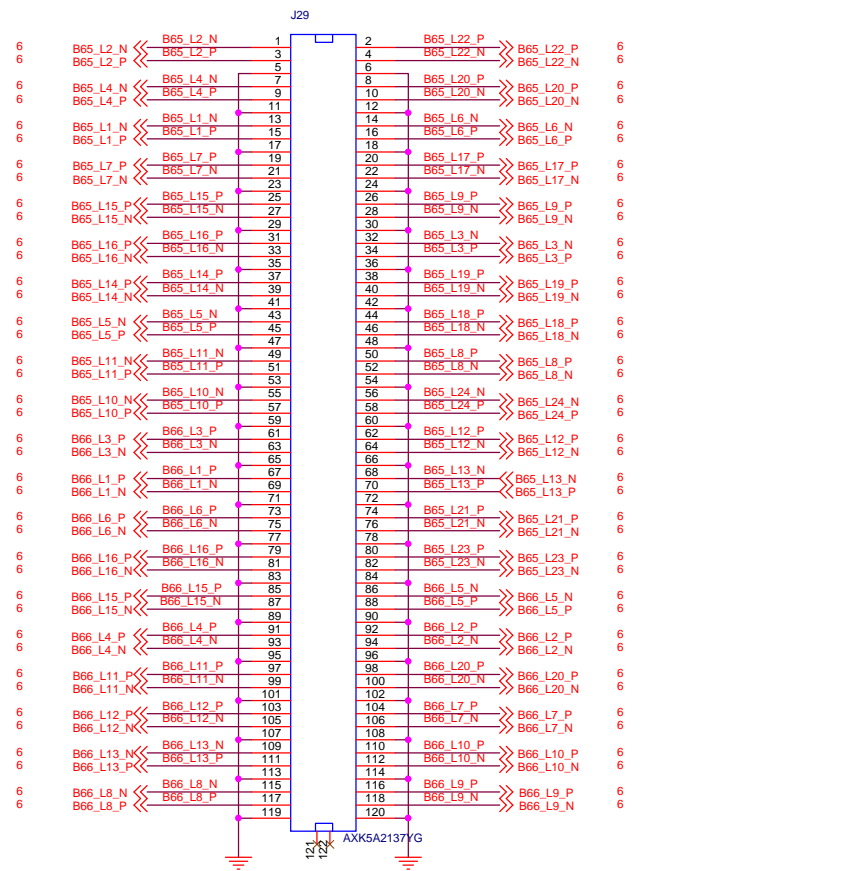
200MHz



PS_IIC1: IIC ADDRESS IS 0x1B

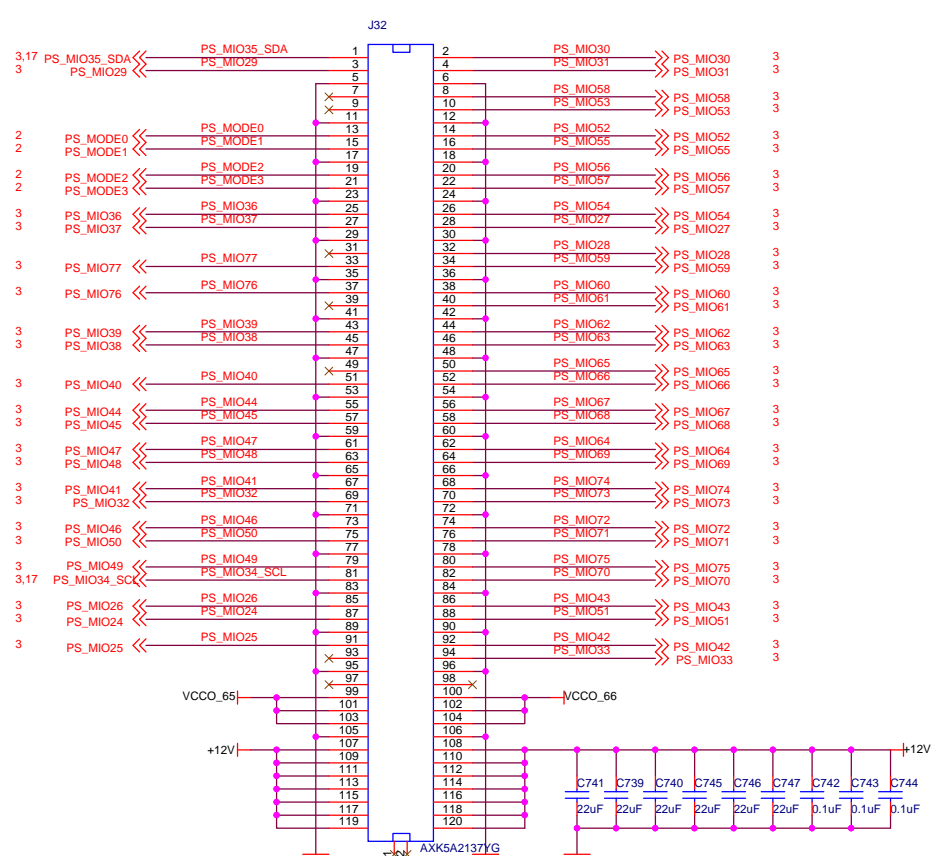
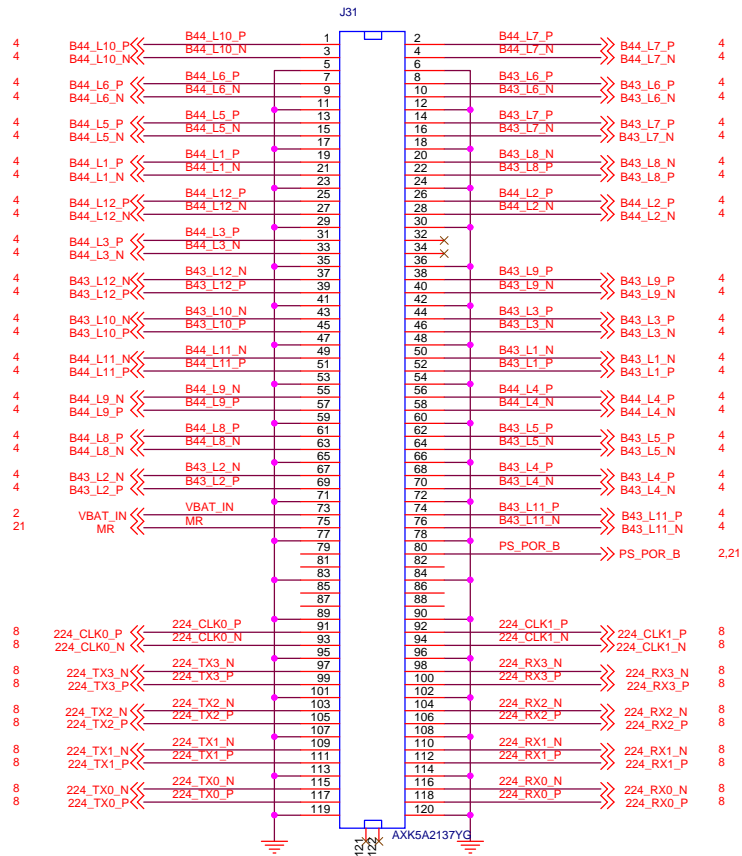
BANK65, BANK66 IO Voltage can not exceed +1.8V

BANK45, BANK46 IO Voltage is +3.3V Standard



BANK43, BANK44 IO Voltage is +3.3V Standard

The MIO Voltage is +1.8V Standard

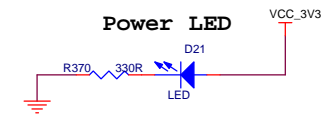
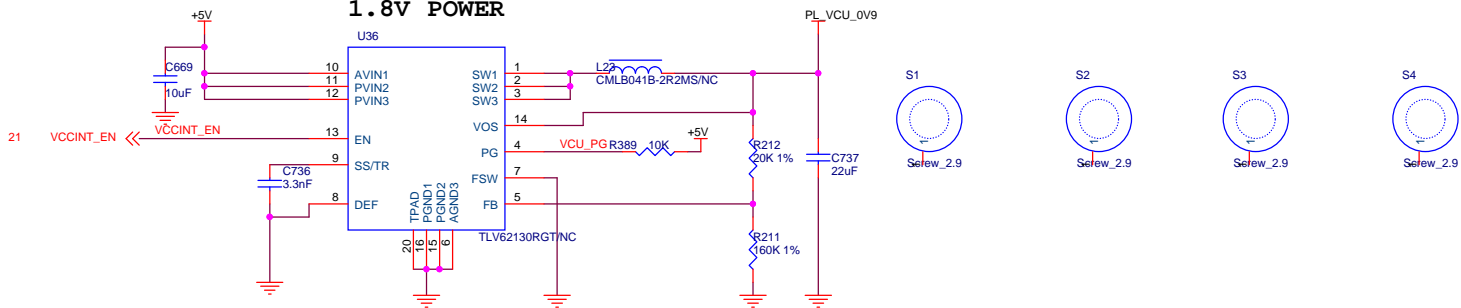


VCCO_65 VCCO_66 Power supply can not exceed 1.8V

POWER ON: VCCINT/VCCINT_IO/VCCBRAM(+0.85V)->VCCINT_VCU(+0.9V)->VCCAUX/VCCAUX_IO(+1.8V)->VCCO(+3.3V, +1.8V)

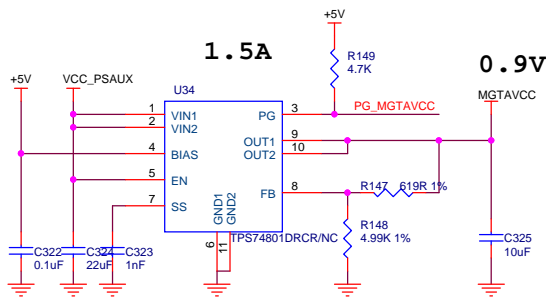
POWER ON: VCCINT(+0.85V)->MGTAVCC(+09V)->MGTAVTT(+1.2V)

1.8V POWER



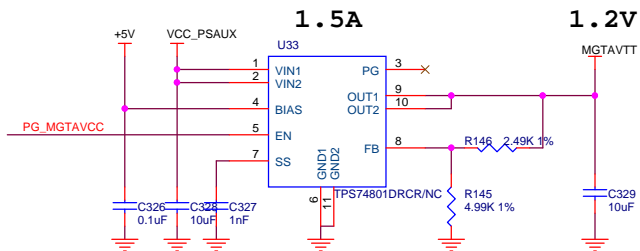
1.5A

0.9V



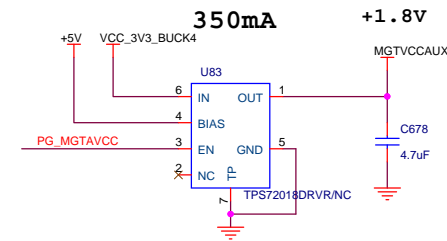
1.5A

1.2V



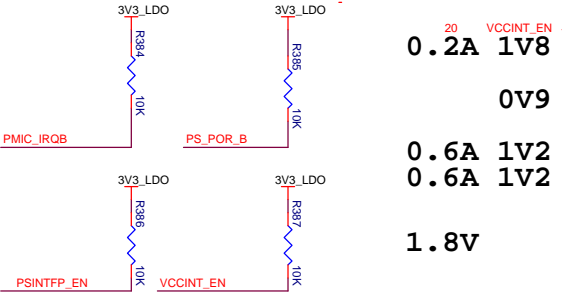
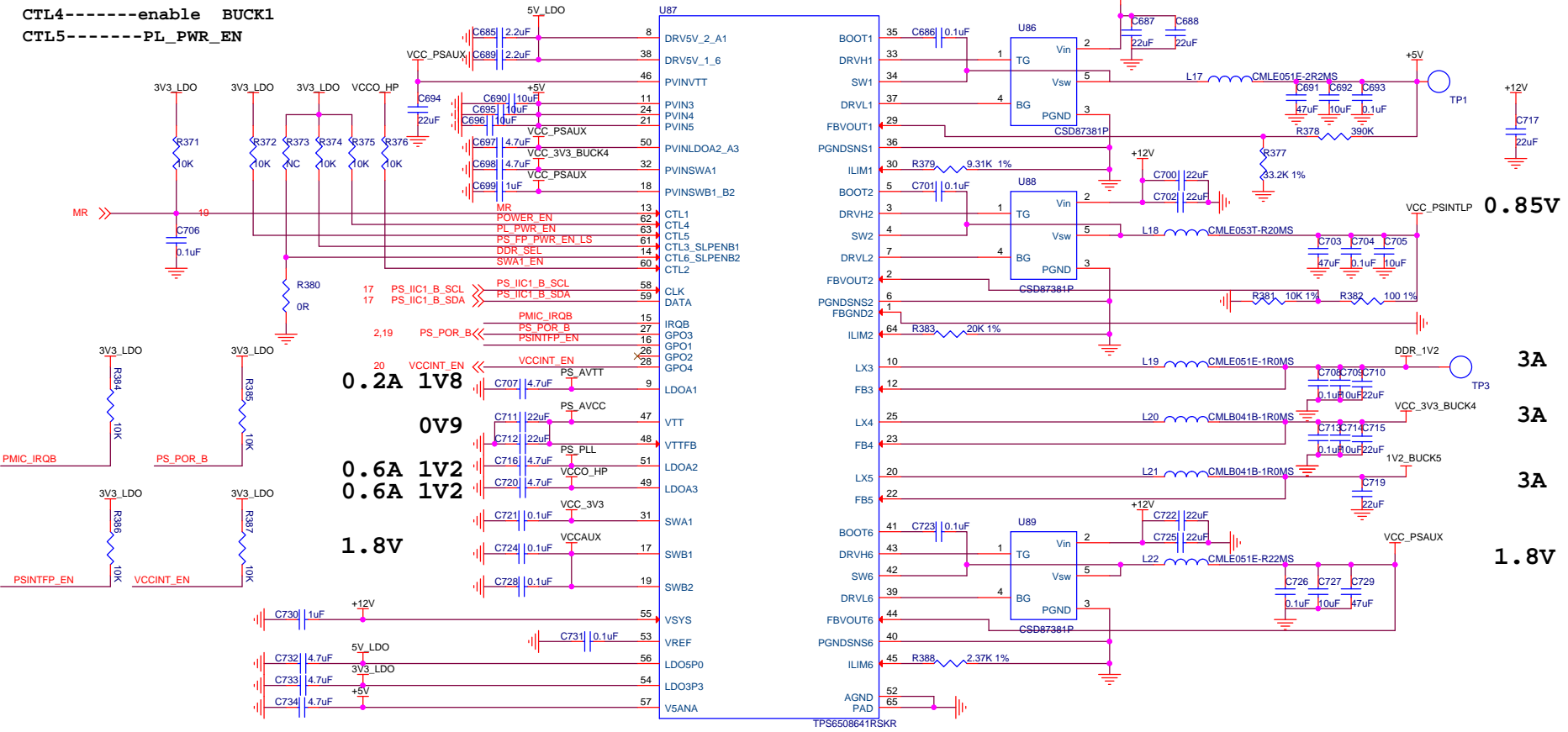
350mA

+1.8V



GPO1-----BUCK1_2_PG
GPO4-----BUCK4_PG

CTL2-----enable and disable SWA1
CTL3-----PS_FP_PWR_EN_LS
CTL4-----enable BUCK1
CTL5-----PL_PWR_EN



PS_IIC0: IIC ADDRESS IS 0x5E

